

**University of Bahrain**  
**College of IT**  
**Department of CE**

**Computer Architecture (ITCE 362)**  
**Academic Year: 2009-2010**  
**Semester: I**  
**Mid Term Exam 2 –Sample Exam**

A

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13-12-2009

|                      |                 |
|----------------------|-----------------|
| <b>Student Name:</b> |                 |
| <b>Student ID:</b>   | <b>Section:</b> |

| Question                 | Points Attached |
|--------------------------|-----------------|
| <b>1 (40 Marks)</b>      |                 |
| <b>2 (20 Marks)</b>      |                 |
| <b>3 (16 Marks)</b>      |                 |
| <b>4 (24 Marks)</b>      |                 |
| <b>Total (100 Marks)</b> |                 |

Q1) Write the abstract and concrete RTN for the following instructions (40 marks)

1- addi ra, rb, c2

|              |                 |                 |
|--------------|-----------------|-----------------|
| Abstract RTN |                 |                 |
| Concrete RTN | Micro-operation | Control Signals |
| T0           |                 |                 |
| T1           |                 |                 |
| T2           |                 |                 |

|    |  |  |
|----|--|--|
| T3 |  |  |
| T4 |  |  |
| T5 |  |  |
| T6 |  |  |

2- shl ra, rb, c2

|              |                 |                 |
|--------------|-----------------|-----------------|
| Abstract RTN |                 |                 |
| Concrete RTN | Micro-operation | Control Signals |
| T3           |                 |                 |
| T4           |                 |                 |
| T5           |                 |                 |
| T6           |                 |                 |
| T7           |                 |                 |

3- not ra, rc

|              |                 |                 |
|--------------|-----------------|-----------------|
| Abstract RTN |                 |                 |
| Concrete RTN | Micro-operation | Control Signals |
| T3           |                 |                 |
| T4           |                 |                 |
| T5           |                 |                 |
| T6           |                 |                 |

Q2) Answer the following:

(20 marks)

I. What is the meaning of the following RTN description? (16 marks)

a-  $Op<4..0> := IR<31..27>$

b-  $M[x]<31..0> := Mem[x]\#Mem[x+1]\#Mem[x+2]\#Mem[x+3]:$

II. What is the meaning of the following RTN notations:

(6 Marks)

| RTN | Meaning |
|-----|---------|
| ;   |         |
| @   |         |
| #   |         |
| :   |         |
| →   |         |
| < > |         |

Q3) Answer the following questions:

I. If the content of r2 is:

(6 Marks)

1001 0111 1110 1010 1110 1100 0001 0110

What is the content of r1 after executing the (**shc r1, r2, 5**) instruction:

- II. Assume that in a certain byte addressing machine all instructions are 32 bits long.  
Assume the following state of affairs for the machine: **(10 Marks)**

| Address | Value |
|---------|-------|
| PC      | 100   |
| r0      | 200   |
| r1      | 300   |
| 100     | 200   |
| 104     | 300   |
| 108     | 400   |
| 200     | 500   |
| 300     | 600   |
| 500     | 700   |

| Instruction      | Addressing Mode | Value of r0 after Execution |
|------------------|-----------------|-----------------------------|
| Load r0, #200    | Immediate       |                             |
| Load r0, 200     | Direct          |                             |
| Load r0, (200)   | Indirect        |                             |
| Load r0, r1      | Register        |                             |
| Load r0, 200[PC] | Relative        |                             |

Q4) Answer The following:

a- Encode the following instructions:

(10 pts)

shra r17, r29, 25

b- Answer with T or F and correct the false:

(10 marks)

- 1- The informal language is better than informal language.
- 2- CISC is newer than RISC
- 3- The effective address for the instruction ld r1, 44(r1) can be calculated by r1+44.
- 4- The abstract RTN description describes the detail execution of an instruction.
- 5- Relative addressing mode uses PC and register.

| Opcode | Value | Opcode | Value |
|--------|-------|--------|-------|
| ld     | 1     | And    | 20    |
| ldr    | 2     | Andi   | 21    |
| st     | 3     | Or     | 22    |
| str    | 4     | Ori    | 23    |
| la     | 5     | Not    | 24    |
| lar    | 6     | shr    | 26    |
| br     | 8     | shra   | 27    |
| brl    | 9     | shl    | 28    |
| add    | 12    | shc    | 29    |
| addi   | 13    | nop    | 0     |

|            |           |             |           |
|------------|-----------|-------------|-----------|
| <b>sub</b> | <b>14</b> | <b>stop</b> | <b>31</b> |
| <b>neg</b> | <b>15</b> |             |           |

| Instruction formats |   |
|---------------------|---|
| 1.                  | <div> <div>31 27 26 22 21 17 16</div> <div>Op   ra   rb   c2</div> <div>0</div> </div>                              |
| 2.                  | <div> <div>31 27 26 22 21</div> <div>Op   ra   c1</div> <div>0</div> </div>   |
| 3.                  | <div> <div>31 27 26 22 21 17 16</div> <div>Op   ra   rc   unused</div> <div>0</div> </div>                          |
| 4.                  | <div> <div>31 27 26 22 21 17 16 12 11</div> <div>Op   rb   rc   (c3) unused   Cond</div> <div>2 0</div> </div>      |
| 5.                  | <div> <div>31 27 26 22 21 17 16 12 11</div> <div>Op   ra   rb   rc   (c3) unused   Cond</div> <div>2 0</div> </div> |
| 6.                  | <div> <div>31 27 26 22 21 17 16 12 11</div> <div>Op   ra   rb   rc   unused</div> <div>0</div> </div>               |
| 7a.                 | <div> <div>31 27 26 22 21 17</div> <div>Op   ra   rb   (c3) unused   Count</div> <div>4 0</div> </div>              |
| 7b.                 | <div> <div>31 27 26 22 21 17 16 12</div> <div>Op   ra   rb   rc   (c3) unused   000000</div> <div>4 0</div> </div>  |
| 8.                  | <div> <div>31 27 26</div> <div>Op   unused</div> <div>0</div> </div>  |